B1 CONT.

wherein the voltage applied to the counter electrode is applied to the supplementary capacitance drive circuit.

REMARKS

Claims 1-20 are pending in the present application; however claims 3, 6, 9, and 14-18 have been previously withdrawn in response to the Applicants' election to prosecute Species I claims. Claim 1, 4, 7, 10, and 19 have been rejected under 35 USC 102(b). Claims 2, 5, 8 and 11-13 have been rejected under 35 USC §103(a). Claim 20 has been newly added.

Applicants herein confirm the previous election to prosecute the Species 1 invention of this application, and reiterate that claims 1, 2, 4, 5, 7, 8, 10-13, 19, and newly added claim 20 are presently directed to and read upon this Species. Applicants further note, however, that, the Examiner, in his Election Requirement, has indicated that claims 1, 4, 7, and 10 are generic. Accordingly, pursuant to 37 CFR 1.141, upon allowance of a generic claim, claims depending therefrom are to be considered with respect to allowability. Applicants respectfully request that the Examiner reaffirm, for the record, that claims 1, 4, 7, and 10 are generic and, moreover, consider withdrawn claims 3, 6, and 9 for allowance as appropriate.

The Applicants appreciate the Examiner's thorough examination of the subject application and respectfully request reconsideration of the subject application based on the above amendments and the following remarks.

35 U.S.C. § 102(b) REJECTIONS

The Examiner has rejected claims 1, 4, 7, 10, and 19 under 35 USC 102(b) as being anticipated by U.S. Patent Number 5,398,043 to Takeda, et al. ("Takeda" or the "Takeda Reference"). The Applicants respectfully traverse the grounds for rejection for the reasons provided below.

The Takeda reference discloses a method for alternating current ("AC") driving an active-matrix liquid crystal display ("LCD") device to improve the image quality due to parasitic capacitance, i.e., charging error. Specifically, "a part of the potential of the modulation signal is changed before the termination of a first ON period of the gate ON signal voltages applied to the TFT." Takeda, col. 3, lines 52-55. As a result, "at least a part of the D.C. components induced by the dielectric anisotropy of the liquid crystal and the scan signal by way of the gate-to-drain capacitance can be compensated [ ]." Id., col. 4, lines 16-19. Accordingly, "no D.C. voltage is applied to the liquid crystal so that a symmetric A.C. drive can be achieved." Id., col. 7, lines 37-38. Indeed,

> A signal [$Ve^{(+)}$ and $Ve^{(-)}$] whose polarity us inverted at every field with respect to the potential of the counter electrode [is supplied] so that it is understood when regarding two fields [i.e., an odd field and an even field] that there is not generated a D.C. electric filed in the potentials at the pixel electrode, signal electrode and counter electrode.

Id., col. 8, lines 2-7 (Emphasis added).

The invention as claimed provides an LCD device and method of driving the same whereby the image is displayed by adjusting the intensity of the transmitted light from the backlight provided on the back surface of the active-matrix substrate, which can deteriorate when a DC bias is applied to the liquid crystal 4, see, e.g., Specification, page 6, lines 6-8, to make leakage-based defects of supplementary capacitances, i.e., bright spots, inconspicuous. See, e.g., Id., page 9, lines 20-21. However, in contrast to Takeda, the present invention recites a "supplementary capacitance drive circuit for driving the supplementary capacitance lines so that a

predetermined potential difference from a voltage applied to the counter electrode is always maintained when any of the pixel electrodes and supplementary capacitance lines leaks." Id., page11, lines 7-10. More specifically, "a predetermined potential difference is maintained from the common signal lines 26." Id., page 26, lines 4-6. As a result of this arrangement, when a leakage defect is caused at the supplementary capacitance 25, the Cs signal that drives the supplementary capacitance lines 23 is applied to the pixel electrodes and the Cs signal has a voltage difference of –2V from the Com signal supplied to the common signal lines 26. See, Id., page 26, line 23 to page 27, line 3.

In short, the Takeda reference does not teach, mention or suggest supplementary capacitance drive circuitry that maintains a predetermined potential difference between supplementary capacitance lines and common signal lines. Instead, according to the Takeda reference, the storage capacitances Cs and the counter electrodes 18 are independently provided for every scan signal wiring 15, and a corresponding modulation signal is applied to each scan signal wiring 15. See, e.g., Takeda, col. 9, lines 1-5. As a result, the pixel potential, which is the voltage applied to the liquid crystal, due to the various voltages and stored capacitances will be as shown as in Takeda FIG. 2(d).

Also, Figure 4 of the Takeda patent shows a modulation circuit 13 that controls voltage on the modulation signal wirings (17a . . . 17z), i.e., supplementary capacitance lines, and a counter potential setting circuit 14 that controls voltage on the counter voltage lines (18a . . . 18z), i.e., common signal lines. Figure 7 of the Takeda patent depicts a counter potential setting circuit 14 for controlling voltage on the counter voltage lines, but the voltage on the supplementary capacitance lines 21a is the same as the scan voltage Vs.

Accordingly, it is respectfully submitted that, the claims are not anticipated by the Takeda reference, and further, satisfy all of the requirements of 35 U.S.C. 100, et seq., especially § 102(b). Accordingly, claims 1, 4, 7, 10, and 19 are allowable.

Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

35 U.S.C. § 103(a) REJECTIONS

The Examiner has rejected claims 2, 5, 8, and 11-13 under 35 USC 103(a) as unpatentable over Takeda. The Applicants respectfully traverse these rejections. For the same reasons provided above that, Takeda, further, does not mention, suggest the invention as claimed.

Accordingly, it is respectfully submitted that, the claims are not made obvious by the Takeda reference, and further, satisfy all of the requirements of 35 U.S.C. 100, et seq., especially § 103(a). Accordingly, claims 2, 5, 8, and 11-13 are allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

If for any reason a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge or credit Deposit Account No. **04-1105**.

Respectfully submitted,

Date: April 16, 2003

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FIG. 10A PRIOR ART

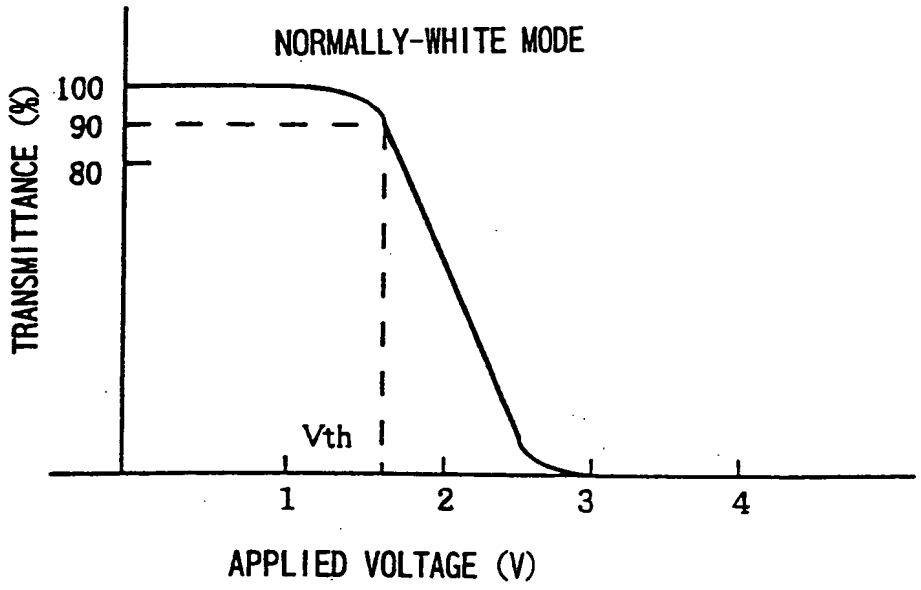

FIG. 10B PRIOR ART